CLAIMS

What is claimed is:

1. An apparatus comprising:

an internal test bus (ITB);

a plurality of deskew clusters coupled to the ITB, wherein the plurality of deskew clusters each include a deskew controller;

an integrated test controller (ITC) coupled to the ITB; and

a debug unit coupled to the ITC;

wherein the ITC generates a single global control signal and the deskew controller generates a first local command signal.

2. The apparatus of claim 1, wherein the plurality of deskew clusters further comprise a plurality of deskew buffers and a regional clock driver (RCD).

3. The apparatus of claim 1, further comprising a second local command signal, wherein the single global control signal and one of the first local command signal, the second local command signal, and both the first local command signal and the second local command signal provide a distributed test control scheme for integrated circuits including debug and testability operations.

4. The apparatus of claim 1, wherein the first local command signal is a snapshot instruction and the second local

command signal is a shift instruction.

5. The apparatus of claim 4, wherein a snapshot instruction can be issued at a first time period and a shift instruction can be issued at a second time period, and results from the snapshot instruction can be shifted by the shift instruction after a third period of time.

6. A method comprising:

generating a single global control signal in an integrated test controller;

decoding the single global control signal in a deskew controller;

generating a first local command signal corresponding to the single global control signal;

distributing the first local command signal to a regional clock driver (RCD); and

performing one of a debug operation and a testability operation on an integrated circuit by using the single global control signal and the first local command signal.

7. The method of claim 6, further comprising generating a second local command signal corresponding to the single global control signal.

8. The method of claim 7, wherein one of the first local command signal is a snapshot instruction and the second local command signal is a shift instruction.

9. The method of claim 8, further comprising issuing a snapshot instruction at a first time period;

issuing a shift instruction at a second time period; and shifting results from the snapshot instruction by the shift instruction after a third period of time.

10. The method of claim 6, further comprising triggering the debug operation after a variable time period.

11. A program storage device readable by a machine comprising instructions that cause the machine to:

generate a single global control signal in an integrated test controller;

decode the single global control signal in a deskew controller;

generate a first local command signal corresponding to the single global control signal;

distribute the first local command signal to a regional clock driver (RCD); and

perform one of a debug operation and a testability operation on an integrated circuit by using the single global control signal and the first local command signal.

12. The program storage device of claim 11, wherein the instructions further cause the machine to:

generate a second local command signal corresponding to

the single global control signal.

13. The program storage device of claim 12, wherein the first local command signal is a snapshot operation and the second local command signal is a shift operation.

14. The program storage device of claim 13, wherein the instructions further cause the machine to: issue a snapshot operation at a first time period;

issue a shift operation at a second time period; and shift results from the snapshot operation by the shift operation after a third period of time.

15. The program storage device of claim 11, the instructions further cause the machine to: trigger the debug operation after a variable time period.